CLAIMS

1. A method for reconfiguring a network of parallel identical functional elements tolerant to the faults of these functional elements, the network comprising said basic functional elements (P), spare functional elements (Sp), interconnecting elements (Cm) of these functional elements, and a control unit, said method being characterized in that it comprises:

- a step of positioning the functional elements of the logic network;
- a routing step of programming interconnecting elements on the physical network, by choosing a maximum number of interconnecting elements which can be passed between two neighbouring processors using a shortest track search algorithm.

2. The method according to claim 1, wherein:

- a network functional element positioning sequence which is composed of a starting functional element and a sequence of functional elements including all functional elements is determined;
- for each of the functional elements, it is positioned tentatively starting with its logical position, then, if required in case of failure, in each of the positions located at a distance 1, distance 2, ... from the logical position of this functional element, a restriction being that one and only one spare position is to be used with respect to the possible positions of previously positioned functional elements, stopping

when S+1 positions have been tested, S being the number of spare functional elements;

- if S+1 positions have been tested without success, returning to the previous functional element in the positioning sequence and proceeding with the next position for this functional element.

3. The method according to claim 2, wherein, when all functional elements have been positioned, it is checked for each network dimension that the logical sequence is followed for each functional element pair, if not, the positions of these functional elements are inverted.

4. The method according to claim 1, wherein the positioning sequence is defined like this: the starting functional element is the top left functional element, the following functional elements are the functional elements to the right and below the starting functional element, and so on, following a diagonal.

5. The method according to claim 1, wherein the network is divided into functional element blocks, and a block positioning sequence is defined starting with a starting block and going through all the blocks from one neighbouring block to the next, the possible positions for the functional elements of one block not including any logical position of the functional elements of previously positioned blocks.

6. The method according to claim 1, wherein the functional elements are processors.

FIGURE 14A

CONFSW_IN OF NEXT Cm

DATA OUTPUT

DATA INPUT

FIGURE 14B

DATA INPUT

ONE OF 6 OUTPUTS

FIGURE 15

NORTH ASIC LINKS

Cm CONTROL

CPU (FPGA)

WEST ASIC LINK

PROCESSOR CONTROL

CONTROLLER

INTEGRITY TESTING

SOUTH ASIC LINKS

EAST ASIC LINK

FIGURE 20/21

LINE INPUT

COLUMN INPUT

RESULTS

FIGURE 4

SET i AND j(i) TO 0 FOR ALL i

ELEMENT i

POSITION j(i) VALID ?

YES

INCREMENT i

END OF POSITIONING?

YES

CORRECT INCONSISTENCIES

END

NO

INCREMENT j(i)

SET j(i) TO 0

INCREMENT j(i-1)

DECREMENT i

FIGURE 10

CM NORTH

P NORTH/EAST

CM EAST

P SOUTH/EAST

CM SOUTH

P SOUTH/WEST

CM WEST

P NORTH/WEST